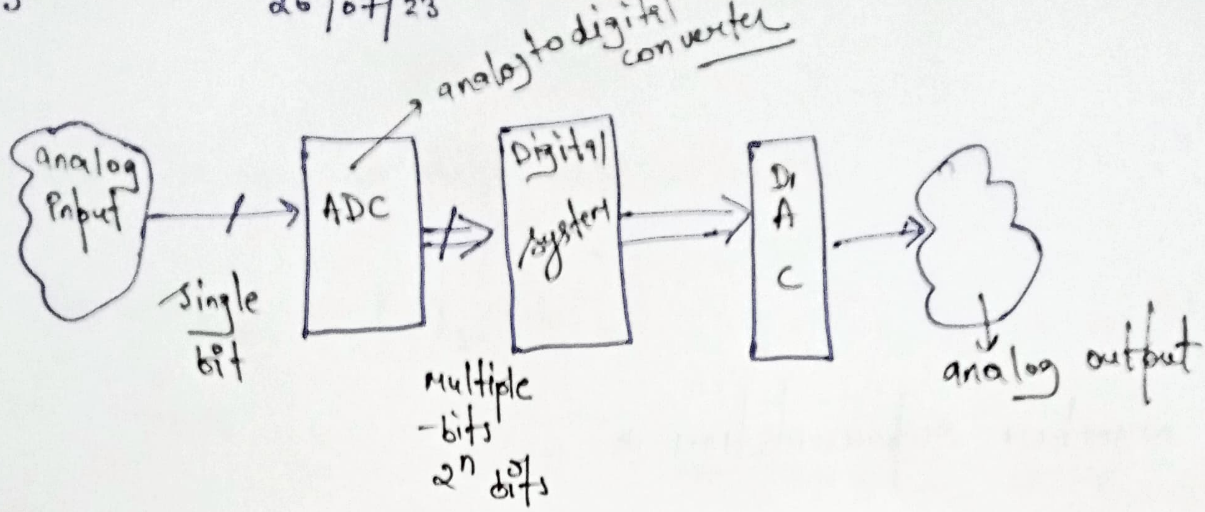
EE203 26/07/23



<u>Digital system</u> →

Computer, Calculator, Digital clock, Digital voltmeter (measurement instrument)

How complex is a system going to be depends on application.

e.g. take recent processor (speed is in GHz and ckt complexity is enormous and for washing machine (controller inside) is less.

Basic Bulding Block of computer →

CPU, Memory
input, output unit

CPU → ALU → ADD, sub, multiplier (Airthemetic)
→ logic, control unit

system → subsystem → Modules

Number representation →

Assumptions

1. we work with voltage (0 to 5V)

'0' → 0V switch off

'1' → 5V switch on

for 3 switch, $2^3 = 8$ level.

for $n = 2$. $= 2^2 = 4$

00 → off off

01 → off ON

10 → ON off

11 → ON ON

to ↑ accuracy ↑ no. of switch.

Digital electronics

conversion a no. in diff base number.

Ex

$$(45.625)_{10} = (?)_2 = (?)_x$$

45   0.625

$x \to 2$		
	45	$\to 1$
2	22	$\to 0$
2	11	$\to 1$
2	5	$\to 1$
2	2	$\to 0$
2	1	$\to 1$

$0.625 \times x \to 2 = 1.250$

$1 \leftarrow = 1.250$

0.250×2

$0 \leftarrow 0.500$

0.500×2

$1 \leftarrow 1.00$

$\to (0.625)_{10}$

$= (0.101)_2$

$$(45)_{10} = (101101)_2 = (231)_4$$

Now $(45.625) = (101101.101)_2$

Binary to decimal system →

$$(101101.101)_2 = (?)_{10}$$

$1\times2^3 \times 1\times2^2 \times \cancel{0\times2^1} + 1\times2^0 \cdot 1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} \ldots$

$\times\, 0\times2^4 \times 1\times2^5$

$32+8+4+1.(0.5+0.125)$

$(45.625)_{10}$

eg. $(231.22)_4 = (?)_{10}$

Binary

$(101101.1010)_2$

or

$2\times4^2 + 3\times4^1 + 1\times4^0 \cdot 2\times4^{-1} + 2\times4^{-2} \ldots$

$32 + 12 + 1 . \frac{2}{4} + \frac{2}{16}$

$= 45.625.$

4

eg

x = Base → allways +ve integer.

$(45)_{10} = (101101)_x$

$45 = x^5 + x^3 + x^2 + 1$

<u>Representation of Number</u> →

⇒ unsigned number eg. +8 = 8 = 1000.

⇒ signed number → used in digit system (micro processor)

eg. +8 = 0 1000 (0 → +ve)

-8 = 1 1000 (1 → -ve)

sign no. ko rep. karne ke liye Extra bit ki jaurat Hogi.

three method to rep signed number.

1) signed magnitude form
2). 1's compliment form
3). 2's compliment form

1's and 2's → for binary (base 2) → (r-1)'s comp. / r's comp.

for decimal → 9's comp / 10's comp

decimal		unsigned	signed		
+0	←	00	00	→	+0
+1	←	01	01	→	+1
+2	←	10	10	→	-0
+3	←	11	11	→	-1

first digit → sign. mag.

1. signed magnitude form →

Eg. $+4 = \underset{\text{sign}}{0}\underset{\text{mag.}}{\underline{100}}$ & $-4 = \underset{\text{sign}}{1}\underset{\text{mag.}}{\underline{100}}$

sign. mag. form

$\underset{+}{0}\underset{\text{mag.}}{\underline{101}} = +5$ & $1101 = -5$.

4 bit

in 8 bit.

4 bit to 8 bit

$+5 = \underset{\text{sign}}{0}\underset{\text{mag.}}{\underline{0000101}}$ & $-5 = \underset{\text{sign}}{1}\underset{\text{mag.}}{\underline{0000101}}$

Range of number →

n=2 bit → 4 binary possible

Binary	Decimal
0 0	+0
0 1	+1
1 0	−0
1 1	−1

Range −1 to 1

= (−1, −0, +0, +1)

for n bit = $\underline{-(2^{n-1}-1) \text{ to } +(2^{n-1}-1)}$

Range.

for n = 3 bit.

Range −3 to +3

= −3, −2, −1, −0, +0, +1, +2, +3.

but for unsigned
0 to +7.

so always we should use signed rep.

Q.. To rep. -4 in signed form how much bit require.

$n=4$ range $= -7$ to $+7$

$n=5$ range $= -15$ to $+15$

to rep. -4 by signed mag. form, minimum 4-bit is required.

$-4 = \underset{4\text{ bit}}{1100} = \underset{8\text{ bit}}{10000100}$

process
or-)

Disadvantage →

1. Two rep. different representation of zero $+0, -0$.
2. Calculation is not easy.

eg.

$x =$ 1100 $= -4$ mini bit $= 4$
0011 $= +3$ min. bit $= 3$

1111 $\;\; -1 = 1001 = 11 = 101$

↓

-7 wrong ans.

liye

1's
comp

comp

now to sol.

$x = -4 = 1100$
$+\; y = -5 = 1101$

$= -9 \qquad 11001.$

↓

min. 5 bit is req.

2). $(r-1)$'s or 1's compliment →

$+x = +x$
$-x = +\bar{x}$

eg. $+x = 0101 = x$
$\overline{+x} = 1010 = \bar{x}$

highest val.

$\bar{x} = 1111$
$- 0101$ ← given val
$\overline{\quad 1010 \quad}$ ↑ $\bar{x}$

let

$x = +4 = 0100$
$\bar{x} = -4 = 1011$ → 4 bit.

8 bit

$\underline{0000}0100$
copy of ↑

$\underline{1111}1011$
copy of ↑

6 bit

000100

6 bit.

111011

In 1's compliment form,
signed magnitude
2's comp.
→ +ve no. = M.S.B = 0
-ve no. = MSB = 1.

Range of 1's Compliment →

for $n = 3$ bit

-3 to 3

$= -3, -2, -1, -0, +0, +1, +2, +3.$

for

n bit = same as signed mag. form.

$-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

• Calculation possible.

disadvantage →

• Two diff rep. of zero i.e. +0 & -0

• Extra addition is req. if carry is generated at time of addition operation.

$(r-1)$'s complement

eg

$(62)_{10} \xrightarrow[\text{comp.}]{9's}$ $\begin{array}{r} 99 \\ -62 \\ \hline 37 \end{array}$, eg $(62)_8 \xrightarrow[\text{comp.}]{7's}$ $\begin{array}{r} 77 \\ -62 \\ \hline 15 \end{array}$

3). 2's complement form → ($\underset{\text{(base)}}{r}$'s compliment). →

$+x = +x$

$-x = \overline{+x} + 1 = 1\text{'s comp.} + 1$

$\left.\begin{array}{l} +7 = 0111 \\ +8 = 01000 \end{array}\right\} \rightarrow$ same as signed and 1's compliment

eg.

$-7 = \overline{+7} + 1 = \overline{0111} + 0001 = 1000 + 0001$

$\boxed{-7 = 1001}$

Binary Number → (2's comp)	decimal no.
00	+0
01	+1
10	−2
11	−1

for $n = 2$ bit.

+ve = +0, +1

−ve = −1, −2

Range of number

$-(2^{n-1})$ to $(2^{n-1}-1)$

$n = 2$ bit = −2 to +1

−2, −1, 0, +1

$n = 4$ bit = −8 to +7.

$(11000)_{2's\ comp} = (?)_{10}$

↓ −ve

$= -x = \overline{+x} + 1 = y$

$+x = +x = y$

$-x = \overline{+x} = y-1$

$x = \overline{y-1}$

$y = 11000$

$y-1 = 11000 - 00001$

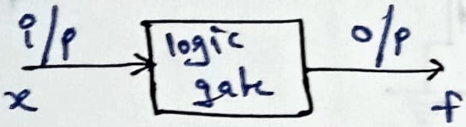
$y-1 = 10111$

$x = \overline{y-1} = 01000$

$\boxed{-x = -8}$

logic gates & Boolean Algebra →

one input logic gate →



$\boxed{y=2}\begin{cases}0\\1\end{cases}$

$\boxed{y=2^n}$ (x)

i/p		o/p		
x	f_1	f_2	f_3	f_4
0	0	0	1	1
1	0	1	0	1
	⇓	⇓	⇓	⇓
	0 (NO)	x	$\bar{x}$	1 → NO logic gate req.

choice req.

four ckt possible.

for n bit input 2^n or 2^{2^n} output possible.

$f \to f_1 = 0$ ✗

$f \to f_2 = x$ = Buffer

$f \to f_3 = \bar{x}$ = not gate

$f \to f_4 = 1$ ✗

1 input gate → Buffer, NOT gate

Buffer

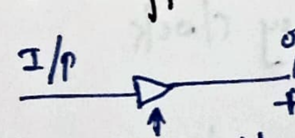
$f = x$

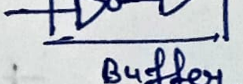
Truth table →

i/p	o/p
x	f
0	0
1	1

- Provide delay $\tau_{p.d.}$
- P.D. = Propagation Delay
- if multipal Buffer are arranged then effective will be sum.

tristate buffer →





Enable E	I/p x	op f
0	0	Hi-Z
0	1	Hi-Z
1	0	0
1	1	1

3 state

11. NOT gate: →

x —▷○— f

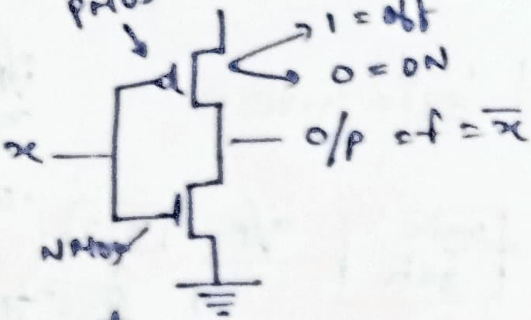
I/p o/p

Truth Table

x	$f = \bar{x}$
0	1
1	0

NOT gate by CMOS: →

PMOS



$x = 0$ PMOS = ON
NMOS = off
$f = 1$

$x = 1$, PMOS = off
NMOS = ON
$f = 0$

1 not gate = 1 PMOS + 1 NMOS
= 1 CMOS
= 2 transistor

if odd No. of NOT gate connected in cascade

x I/p —▷○—▷○— . . . . —▷○— o/p $f = \bar{x}$

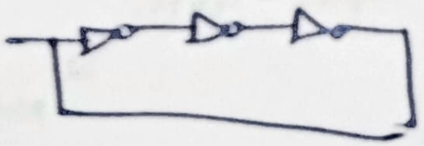
⇓

x —▷○— $f = \bar{x}$

i/p o/p

$t = n \cdot \tau_{pd}$
↑
odd

sequential clct

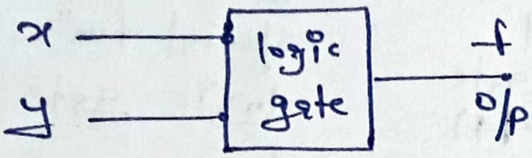


↑
Square wave

frequency clock

$$f_{clk} = \frac{1}{T_{clk}} = \frac{1}{2 \times n \times \tau_{pd}}$$

2 input logic gate



Boolean ~~functions~~ functions
$2^{2^n} = 16.$

→ 2 donot rep: logic gate
→ 10 logic gate

10th logic gate

- $A \cdot B$ = AND gate
- $\bar{A}B + A\bar{B}$
  $= A \oplus B$ = X-OR gate
- $A + B$ = OR gate
- $\bar{A} \cdot \bar{B} = \overline{A+B}$ = NOR gate
- $A \cdot B + \bar{A} \cdot \bar{B}$
  $A \odot B$ = X-NOR gate
- $\bar{A} + \bar{B}$
  $\overline{A \cdot B}$ = NAND gate

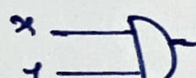
A	B	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}	f_{16}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		0	$A \cdot B$	$A \cdot \bar{B}$	A	$\bar{A} \cdot B$	B	$\bar{A}B + \bar{B}A$	$A+B$	$\bar{A}\bar{B}+AB$ → f_{10}; $\bar{A} \cdot \bar{B}$		$\bar{B}$	$A+\bar{B}$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$	1

2 input logic gates.

logic gate

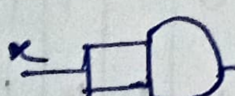
- Basic logic gate (3 or 4)
  - 1 input
    - NOT
    - Buffer
  - other 2 input
    - OR
    - AND
- universal logic gate (2/4)
  - NAND
  - NOR
  - $A\cdot\bar{B}$, $\bar{A}\cdot B$
  - $A+\bar{B} \rightarrow \bar{A}+B$
- special fun" logic gate
  - X-OR (unequality gate)
  - X NOR (equality gate)

AND gate

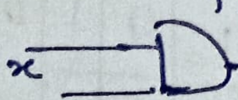


x	y	f = x·y
0	0	0
0	1	0
1	0	0
1	1	1

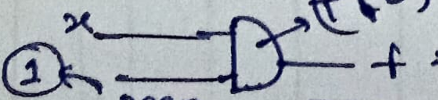
Majority i/p = 0



Buffer

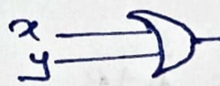


Buffer.



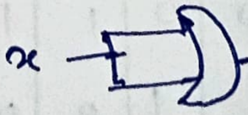
open → ''is
(floting terminal) design by
Can not defined. CMOS then output

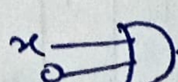
OR gate

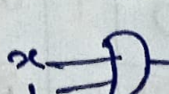


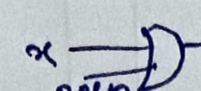
x	y	f = x+y
0	0	0
0	1	1
1	0	1
1	1	1

Majority i/p = 1.



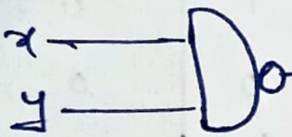
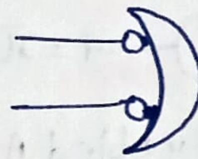






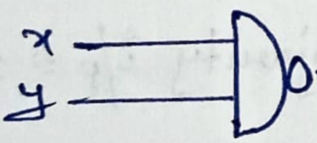
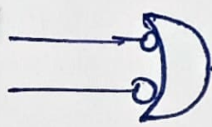
Universal logic gate

1.* NAND gate →
(AND + NOT)


$f = \overline{A \cdot B} = \bar{A} + \bar{B}$

$f = \bar{A} + \bar{B} = \overline{A \cdot B}$

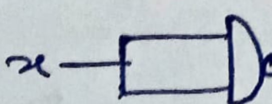
Bubbled (NOT) + OR

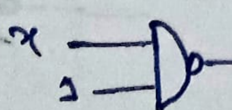
Bubbled OR gate

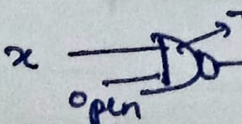

f =

f

x	y	$f = \overline{x \cdot y} = \bar{x} + \bar{y}$
0	0	1
0	1	1
1	0	1
1	1	0

Majority input = 0 = AND gate (also).
⇓ o/p ⇓ 1.
↓ Here o/p ⇓ 0


$f = \bar{x}$

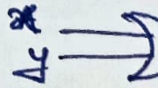

$F = \bar{x}$



$f = \bar{x}$

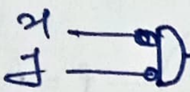

$f = 1.$

2. NOR gate (OR + NOT) →



$f = \overline{x+y} = \bar{x} \cdot \bar{y}$

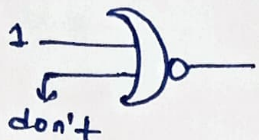
or



$f = \bar{x} \cdot \bar{y}$

Bubbled AND

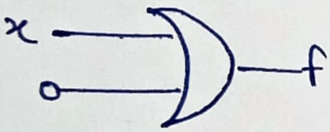
x	y	$f = \overline{x+y} = \bar{x} \cdot \bar{y}$
0	0	1
0	1	0
1	0	0
1	1	0



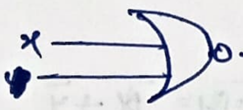
$f = 0$

Majority i/p = 1.

$f = \bar{x}$



$f = \bar{x}$

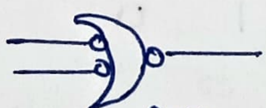


$f = 0$

$\boxed{\text{OR} = \text{NOR} + \text{NOT}}$

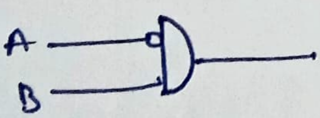
$\boxed{\text{AND} = \text{NAND} + \text{NOT}}$

OR

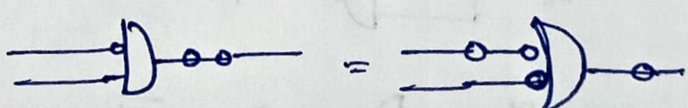


AND

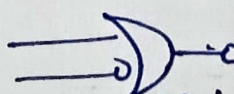
3. global 1 ($A \cdot \bar{B}$)



$f = \bar{A} \cdot B$

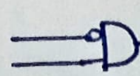


≡



OR

≡



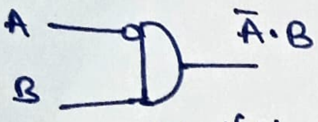
AND

A	B	$f = \bar{A} \cdot B$
0	0	0
0	1	1
1	0	0
1	1	0

Majority i/p = NO

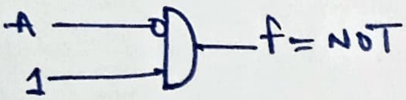
Can not defined

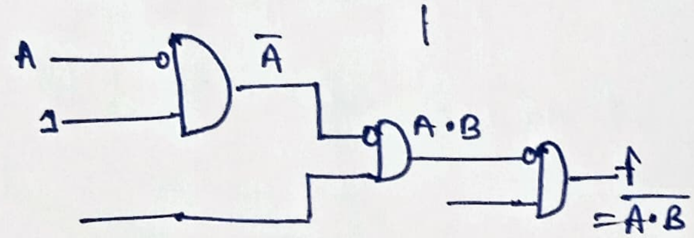
NAND gate by global '1' →



$$NAND = \overline{A \cdot B} = \bar{A} + \bar{B}$$

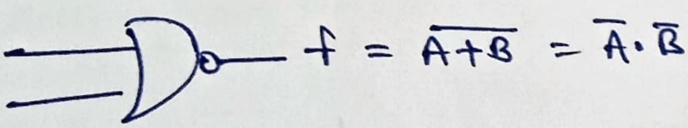
=



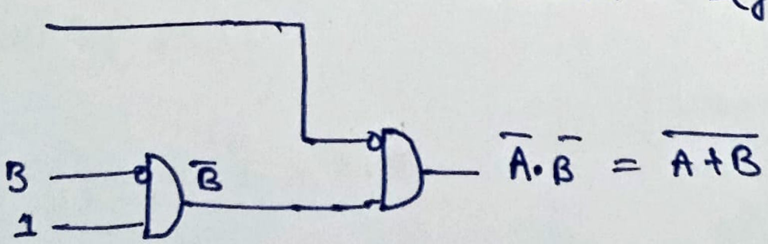


NAND = 3(global '1')

NOR gate by global '1' →



NOR = 2(global '1')



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Special logic gates:→

- EX-OR = XOR $\Rightarrow f = A \oplus B \rightarrow \bar{A}B + A\bar{B}$
- X NOR $\quad f = A \odot B \rightarrow AB + \bar{A}\bar{B}$

(5*)

$$XNOR = \overline{XOR}$$

$$XOR = \overline{XNOR}$$

Buffer = $\overline{NOT}$

AND = $\overline{NAND}$

OR = $\overline{NOR}$

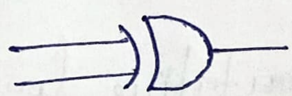
A	B	$A \oplus B$	$A \odot B$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

$A \oplus B$ ↓ in equality detector

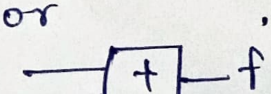
$A \odot B$ → equality detector.

$A \oplus B$: if { odd 1 ⇒ 1, even = 0. }

$\boxed{XOR}$



or



$f = A \oplus B$

Boolean Algebra →

Boolean principle →

1. Demorgans low → $\bar{\bar{A}} = A$, $\bar{\bar{x}} = x$

$$\overline{x \cdot y} = \bar{x} + \bar{y}$$

$$\overline{x + y} = \bar{x} \cdot \bar{y}$$

2. Idempoting low →

$x + x = x$; $x \cdot x = x$

$1 + 1 = 1$; $1 \cdot 1 = 1$

$0 + 0 = 0$; $0 \cdot 0 = 0$

$x (NAND) x = \bar{x}$ | $x (NOR) x = \bar{x}$

3. Commutative low →

$x + y = y + x$; $x (NAND) y = y (NAND) x$

$x \cdot y = y \cdot x$; $x (NOR) y = y (NOR) x$

4. Associative low →

$(x + y) + z = x + (y + z)$

$(x \cdot y) \cdot z = x \cdot (y \cdot z)$

NAND & NOR do not follow associative low.

5. Compensation low →

$x + \bar{x} = 1$; $x (NAND) \bar{x} = 1$

$x \cdot \bar{x} = 0$; $x (NOR) \bar{x} = 0$

NOT low extra.

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6. Distributive low →

$$x(y+z) = xy + xz$$

$$x + yz = (x+y)(x+z)$$

7. Absorbtion low →

$$x + x'y = \cancel{(x+x')}(x+y) = x+y$$

$$x + xy = (x+x)(x+y) = x(1+y) = x$$

8. Consensus low →

$$xy + x'z + yz = xy + x'z$$

$$xy' + xz + yz = xy' + yz$$

9. Duality principle →

AND $\xrightarrow{Dual}$ OR, NAND $\xrightarrow{Dual}$ NOR

Dual: 0 → 1, 1 → 0

+ve level logic: 1 → high, 0 → low

−ve level logic: 1 → low, 0 → high

$f(x,y) = \overline{x \cdot y}$

$f_D(x,y) = \overline{x+y}$

$f'(x,y) = x \cdot y$

AND का OR करो only.

+ve level logic c/t $\xrightarrow{Dual}$ −ve level logic

$f(x,y) = \overline{x+y}$

$f'(x,y) = x+y$

$f_D(x,y) = \overline{x \cdot y}$

OR को AND में Con

10. Complement of fun"

let $f(x,y,z) = xy + yz + xz$

to compliment in Boolen alz. — and to or, or to and and compliment of each variable.

$$f'(x,y,z) = (\bar{x}+\bar{y}) \cdot (\bar{y}+\bar{z}) \cdot (\bar{x}+\bar{z})$$

Canonical form →

Minterms → [standard product term]

	x	y	minterms = 1
	0	0	0 → x'y'
1 →	0	1	1 → x'y
2 ←	1	0	1 → xy'
	1	1	0 → xy

$f(x,y) = \Sigma_m (1,2) = \Sigma(1,2)$

SOP $= x'y + xy'$

$\boxed{\text{SOP} = \text{AND-OR Ckt}}$

$\boxed{\text{SOP} = \text{NAND-NAND Ckt}}$

Maxterms: [standard sum term] →

x	y	Maxterm = 0	
0	0	0	x+y → 0
0	1	1	x+y' → 1
1	0	1	x'+y → 2
1	1	1	x'+y' → 3

$f(x,y) = \Pi M(0,3)$

$= (x+y)(x'+y')$

$\boxed{\text{POS}}$ → product of sum

$\boxed{\text{POS} = \text{OR-AND Ckt}}$

$\boxed{\text{POS} = \text{NOR-NOR Ckt}}$

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Que.

$f(x,y,z) = xy + yz + xz$

write down SOP & POS form of this boolean funⁿ.

Sol

$f(x,y,z) = xy(z+z') + (x+x')yz + x(y+y')z$

$= xyz + xyz' + xyz + x'yz + xyz + xy'z$

$= xyz + xyz' + x'yz + xy'z$

$\quad \downarrow \qquad \downarrow \qquad \downarrow \qquad \downarrow$

$\quad 7 \qquad 6 \qquad 3 \qquad 5$

$f(x,y,z) = \Sigma_m(3,5,6,7)$

$\Pi_M(0,1,2,4)$

$f'(x,y,z) = \Sigma_m(0,1,2,4)$

$\Pi_M(3,5,6,7)$

another simple way →

$f(x,y,z) = xy + yz + xz$

$\downarrow$

$11t + t11 + 1t1$

$110 \quad 111 \quad 011 \quad 111 \quad 101 \quad 111$

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$6 \quad 7 \quad 3 \quad 7 \quad 5 \quad 7$

$\Rightarrow f(x,y,z) = \Sigma_m(3,5,6,7)$

Que. $f(x,y,z) = (x+z')(y'+z')(x'+y)$ Sol. for Connical form

Sol

$f(x,y,z) = (x + y\cdot y' + z')(x\cdot x' + y' + z') + (x' + y + zz')$

$= \underbrace{(x+y+z')}_{001}(\underbrace{x+y'+z'}_{011}) + \underbrace{(x+y'+z')}_{011}\underbrace{(x'+y'+z')}_{111}$

$+ \underbrace{(x'+y+z)}_{100}\underbrace{(x'+y+z')}_{101}$

$\pi_M(1,3,4,5,7)$

$\Sigma_M(0,2,6)$

Note this is Maxterm

$x \to 0$

$x' \to 1$

but in minterm

$x \to 1$

$x' \to 0$

another simple way →

$f(x,y,z) = (x+z')(y'+z')(x'+y)$

0.y.1		x 1 1		1 0 z	
001	011	011	111	100	101
1	3	3	7	4	5

$\pi_M(1,3,4,5,7)$

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• How to process any boolean fun" from logic gates:→

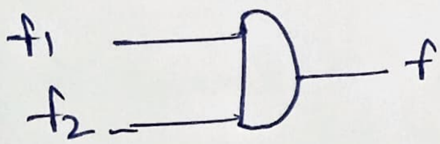
→ **NOT gate** →

$f(x,y,z)$ $\quad$ $f'(x,y,z)$

$= \Sigma m(1,2,4,7)$ $\quad$ $= \Sigma m(0,3,5,6)$

$= \pi M(0,3,5,6)$ $\quad$ $\pi M(1,2,4,7)$

→ **AND gate** →



$f_1(x,y,z) = \Sigma(1,2,3,4,7)$ $\quad$ $f(x,y,z) = ?$

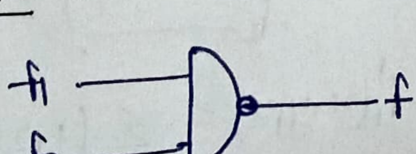
$f_2(x,y,z) = \Sigma(0,1,4,6)$

Sol: comman term will be answer.

$$f(x,y,z) = \Sigma(1,4) = \pi(0,2,3,5,6,7) = g(x,y,z)$$

NOT POS (πM) से comman नहीं लेना है।

→ **NAND gate** →

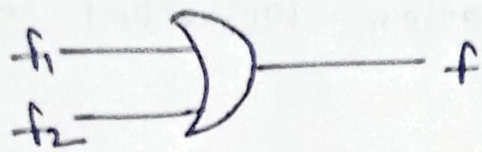


$f_1(x,y,z) = \Sigma(1,2,3,4,7)$ $\Rightarrow$ $g(x,y,z) = \Sigma(1,4)$

$f_2(x,y,z) = \Sigma(0,1,4,6)$ $\quad$ $f(x,y,z) = \pi(1,4)$

$= \Sigma(0,2,3,5,6,7)$

OR gate →



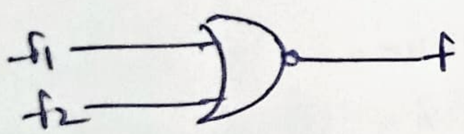
$f_1(x,y,z) = \Sigma(0,2,3,6,7)$

$f_2(x,y,z) = \Sigma(1,2,6)$ $\boxed{SOP}$ → sum of both f_1 & f_2.

$f(x,y,z) = \Sigma(0,1,2,3,6,7) = g[x,y,z]$

NOTE MAXTERM (πM) में add नहीं करना

NOR gate →



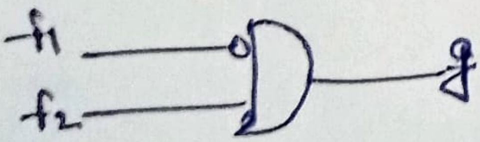
$f_1(x,y,z) = \Sigma(0,2,3,6,7)$

$f_2(x,y,z) = \Sigma(1,2,6)$

$g(x,y,z) = \Sigma(0,1,2,3,6,7)$

$f(x,y,z) = \Sigma(4,5) = \pi(0,1,2,3,6,7)$

Global 1



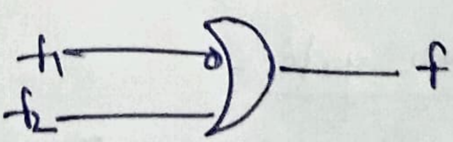
$f_1(x,y,z) = \Sigma(0,3,5,6)$

$f_2(x,y,z) = \Sigma(0,1,2,6)$

$g(x,y,z) = \Sigma(1,2)$

$= \pi(0,3,4,5,6,7)$

Global 2



$f_1(x,y,z) = \Sigma(1,2,4,7)$

$f(x,y,z) = \Sigma(0,1,2,4,6,7)$

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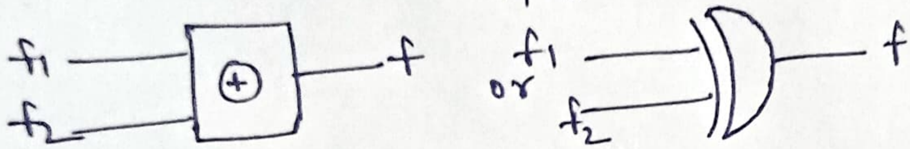
X-OR gate

$f_1\bar{f_2} + \bar{f_1}f_2$



$f_1(x,y,z) = \Sigma(0,1,6,7)$ $\quad f_1'(x,y,z) = \Sigma(2,3,4,5)$

$f_2(x,y,z) = \Sigma(0,1,2,3,4,5)$ $\quad f_2'(x,y,z) = \Sigma(6,7)$

$f(x,y,z) = \Sigma(6,7) + \Sigma(2,3,4,5)$

$= \Sigma(2,3,4,5,6,7) = \pi(0,1)$

Sol जो दोनों में comman है और जो नहीं है उन्हे छोड़ दो।

But this is the solⁿ for XNOR